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09/750,090	12/29/2000	Jeffery F. Harness	2207/10377	6380

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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/750,090
Filing Date: December 29, 2000
Appellant(s): HARNESS ET AL.

Jeffrey F. Harness, et al.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 11/26/2007 appealing from the Office action mailed 06/23/2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,034,744	Obinata	7-1991

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The rejection of claims 1, 7, 10, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,034,744 to Obinata ("Obinata").

The rejection of claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obinata.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 7, 10, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Obinata (U.S. 5,034,744).

Re claim 1, Obinata discloses in Figure 1 a method of filtering over-sampled data (e.g. abstract and col. 2 lines 35-63 wherein circuit in Figure 1 is used to filter-out as suppress the digital glitch(es) of the over-sampled data from filter circuit 20) comprising:

a. receiving (e.g. Figure 1 as outputting over-sampled data from component 20 to S/P converter 23) a word of over-sampled data including a plurality of sample bits for each of a plurality of data bits (e.g. col. 3 lines 57-63 and Figure 2(a) wherein each world contains series of bits from LSB to MSB as seen in Figure 2(a));

b. detecting (e.g. col. 2 lines 46-62; col. 3 lines 37-41 as definition of glitch(es); and top portion of Figure 1) a sample bit having one logic value and, adjacent bits on both sides of said sample bit each having an opposite logic value to the one logic value of said sample bit (e.g. col. 2 lines 46-55; col. 3 lines 37-41 as definition; col. 5 lines 31-48; and to suppress the glitch(es), the circuit as seen must detect the glitch(es) with different raise or fall edge by the AND gates 40 and 41); and

c. outputting (e.g. output of Figure 1) the received word with the sample bit having said one logic value inverted (e.g. abstract and col. 5 lines 37-48 wherein once the detection is high as glitch occurs, the inverter would enable to flip or suppress the glitch logic).

Re claim 7, Obinata further discloses in Figure 1 over-sampling data and receiving word from at least one over-sampler (e.g. part 20 in Figure 1 and col. 3 lines 57-63).

Re claim 10, it is an apparatus claim of claim 1. Thus, claim 10 is also rejected under the same rationale in the rejection of rejected claim 1.

Re claim 19, it is a computer readable memory containing program instruction claim of claim 1. Thus, claim 19 is also rejected under the same rationale in the rejection of rejected claim 1.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Obinata (U.S. 5,034,744).

Re claims 8-9, Obinata does not disclose in Figure 1 a step of receiving word from an over-sampler or between two over-samplers wherein the over-sampled data is USB 2.0 data. However, the examiner takes an official notice that the technique of selecting data from multiple input source as over-samplers and USB 2.0 data are well-known in the art of technology.

Therefore, it would have been obvious application to a person having ordinary skill in the art at the time the invention is made to apply difference data as USB 2.0 or samplers into Obinata's invention because it would enable to correct any undesirable sequence or irregular sequence and provide a desired sequence without loss of integrity (e.g. col. 1 lines 10-20 and col. 2 lines 43-62).

(10) Response to Argument

I. The applicant argues in pages 5-8 for claims 1, 10, and 10 rejected under 35 U.S.C. 102(b) as being anticipated by Obinata (U.S. 5,034,744) as Obinata does not teach or suggest features cited in the claimed invention, particularly the step of detecting a sample bit having one logic value and adjacent bits on both sides of sample bit.

A. The applicant argues in page 5 last paragraph to first paragraph page 6 that even though the cited reference by Obinata discusses the detection of "status changes", but fails to clearly suggest a step of detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit having an opposite logic value since Figure 1 is made to compare the sample bit and the previous sample bit.

The examiner respectfully submits that the cited reference by Obinata discloses, logically and reasonably, the step of "detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit having an opposite logic value" as stated in the abstract, col. 2 lines 46-55, col. 3 lines 37-45, and finally col. 5 lines 30-48. The Obinata's objective is to remove/suppress the glitches in the input data wherein the glitch(es) is defined as the value of a bit is changed from one level to another level as seen in col. 3 lines 37-41 with positive glitches occur at "1" to "0" and negative glitches occur at "0" to "1". In order to remove or suppress the glitch bit(s), the glitch(es) must be detected by detecting the changes in digital logic level in order to distinct the glitch(es) from regular data. The detection of logic level changes is done by mainly top portion of Figure 1 and particularly addressed in col. 5 lines 31-45 in detail. In this paragraph, the positive glitch is identified and eliminated by detecting the changes of logic level. The detection of difference logic level from the first side of glitch is done in col. 5 lines 31-33 for detecting difference logic level from "0" to "1" and stored to AND gate 40 as "H". The detection of difference logic level from the second side of glitch is done in col. 5 lines 33-36 for detecting difference logic level from "1" to "0" and stored to AND gate 41 as "H". These values of AND gates are later used to enable an inverting means for removing/suppressing the glitch if both of AND gates are "H". Thus clearly, the cited reference by Obinata discloses the step of "detecting a sample bit having one logic value and adjacent bits on both sides of the sample bit having an opposite logic value" as above argued by the applicant.

B. The applicant further argues in pages 6-7 that the detection of "status changes" is the situation where a previously sampled bit is different from a current sample bit, not to adjacent bits on both sides of the sample bit as required by the claimed invention.

The examiner respectfully submits that the previous sample bit can be considered as the adjacent bit respective to the sample bit wherein the sample bit is the current sample bit and the adjacent bits are the previous and advance bit relative to the current sample bit. Thus, there is no difference between the current claimed invention and the cited reference.

II. The applicant argues in page 8 last paragraph for claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable by Obinata (U.S. 5,034,744) since feature of independent claim 1 is neither shown, explicitly or inherently, by Obinata and is not obvious in view of Obinata, the reversal of rejection under 35 U.S.C. 103(a) is respectfully requested.

The examiner respectfully submits that the examiner has clearly addressed in the above rejection and responses to the argument how the cited reference by Obinata discloses every limitations of independent claims and further how it is obvious/unpatentable in view of Obinata for dependent claims. In addition, the applicant does not clearly state how and why it is not obvious in view of Obinata for dependent claims 8-9. Thus, claims 8-9 are firmly rejected under 35 U.S.C. 103(a) as being unpatentable over Obinata (U.S. 5,034,744).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

January 14, 2008

Chat C. Do

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